

ABSTRACT

A method and apparatus for improving the performance of a memory wordline decoder is disclosed. A decoder latch is attached to an inverter which drives the wordline. Additionally, a voltage pump can supply operating voltage to the inverter to assist in overdriving the wordline. A voltage sink can also be coupled to the inverter which, in combination with the voltage pump, can be used to shift the output voltages used to turn the wordline on and off. A second inverter can also be added, and in such a case the transistors within the latch and the first inverter can be reduced in size, switching time, and power consumption.